Amendments to the Claims:

1 - 6 (Canceled)

7. (Currently amended) ~~The invention as defined in claim 1~~ A method of determining when a frame of information comprised of one or more data buffers of information being transmitted in a network processor has completed transmission by a transmission system therein, comprising the steps of:

providing a plurality of buffer control blocks, each having space for control information to link one buffer to another for transmitting information in each data buffer,

each of said buffer control blocks having a last bit flag bit having a first position wherein an additional data buffer is to be chained to a previous data buffer and a second position wherein no additional data buffer is to be chained to a previous buffer wherein each buffer control block includes the next buffer address when the last big flag bit is in either the first position or the second position; and

supplying the position of said last bit flag bit in each buffer control block to the transmission system of said network processor.

8. (Original) The invention as defined in claim 7 wherein said next buffer address corresponds to the address of the next buffer control block and the next data buffer.

9 - 14 (Canceled)

15. (Currently amended) ~~The invention as defined in claim 10~~ A plurality of buffer control blocks for use in controlling the transmission of buffers of data in a frame in a network processor, comprising:

each buffer control block having space for control information to link one buffer to another for transmitting information in each data buffer;

each of said buffer control blocks having a last bit flag bit having a first position wherein an additional data buffer is to be chained to a previous data buffer and a second position wherein no additional data buffer is to be chained to a previous buffer wherein each buffer control block includes the next buffer address when the last big flag bit is in either the first position or the second position.

16. (Original) The invention as defined in claim 15 wherein said next buffer address corresponds to the address of the next buffer control block and the next data buffer.

17. (Canceled)

18. (Previously presented) A method of determining when a frame of information comprised of one or more data buffers of information being transmitted in a network processor has completed transmission by a transmission system therein, comprising the steps of:

providing a plurality of buffer control blocks, each having space for control information to link one buffer to another for transmitting information in each data buffer,

wherein the control blocks are in a free buffer control block queue when not in use in conjunction with a data buffer,

each of said buffer control blocks having a last bit flag bit having a first position wherein an additional data buffer is to be chained to a previous data buffer and a second position wherein no additional data buffer is to be chained to a previous buffer;

wherein said last big flag bit is in said second position when in the free buffer control block queue, wherein said last big flag bit in each buffer control block is flipped to the first position when said control block buffer has written therein a starting and ending address for the next data buffer; and

supplying the position of said last bit flag bit in each buffer control block to the transmission system of said network processor.

19. (Previously presented) A plurality of buffer control blocks for use in controlling the transmission of buffers of data in a frame in a network processor, comprising:

each buffer control block having space for control information to link one buffer to another for transmitting information in each data buffer;

wherein the control blocks are in a free buffer control block queue when not in use in conjunction with a data buffer;

each of said buffer control blocks having a last bit flag bit having a first position wherein an additional data buffer is to be chained to a previous data buffer and a second position wherein no additional data buffer is to be chained to a previous buffer wherein said last bit flag bit is in said second position when in the free buffer control block queue, and

wherein said last bit flag bit in each buffer control block is flipped to the first position when said control block buffer has written therein a starting and ending address for the next data buffer.